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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/594,556	06/15/2000	Naoya Wada	193130US2X	8640

7590 12/28/2004

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EXAMINER	
BELLO, AGUSTIN	
ART UNIT	**PAPER NUMBER**
2633	

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/594,556	WADA ET AL.	
	Examiner	Art Unit	
	Agustin Bello	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/27/04 AND 8/27/04*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *3 and 9-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 3 and 9-21 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 8/27/04.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Araki in view of U.S. patent No. 5,729,548 to Holender.

Regarding claim 1, Araki discloses a photonic network packet routing method (Fig. 1 or Fig. 20) comprising a step of discriminating (e.g. extracting) the encoded address information of the IP packet (Col. 12, lines 33-36) by optical correlation processing (e.g. via 105, 107, 109 and 110 of Fig. 2 and via 503 and 525 of Fig. 1 1), a step of switching to an output path (e.g. via combination of 103, 104 and 100 of Fig. 1) for the IP packet based on a result of the discrimination (e.g. via 1003 and 1004 of Fig. 2 and Col. 12, lines 37-50), and a step of outputting the IP packet labeled with prescribed address information (e.g. Destination 1 of input unit of Fig. 25 and 2003 of Fig. 24 and Col. 1 1, lines 37-44) on the output path selected by the switching step (Col. 10, lines 39-47 and Col. 1 1, lines 1 1-21). Though he discloses a step of

encoding address information (e.g. 950 of Fig. 30) using light attributes (1001 of Fig. 30), he fails to disclose a step of optically encoding destination address information attached to an IP packet. Holender discloses an optical encoder (optically encoding) (916 of Fig. 9) for encoding optical pattern that corresponds to the destination's address (destination address information) (Col. 2, lines 24-52 and Col. 15, lines 39-48) attached with packet payload (913 of Fig. 9) and packet address (912 of Fig. 9). Accordingly, one of the ordinary in the art would have been motivated to incorporate an optical encoder for optically encoding address information to increase the speed of telecommunications switches by adapting optical encoding-decoding techniques to telecommunications applications. Therefore, it would have been obvious to one of artisan skill in the art to have modified the optical packet switching system of Araki by substituting the steps of encoding address information with steps of encoding address information using optical encoders as taught by Holender to obtain the invention as claimed in claim 1.

4. Regarding claim 4, Araki in view of Holender discloses discrimination of the optically encoded address information (e.g. via 916 of Fig. 9, Holender) is conducted by sending the IP pack, et (e.g. 1001 of Fig. 11, Araki labeled with address information (e.g. via 1003 or 525 or 1002 of Fig. 1 1, Araki or via 912 of Fig. 9, Holender) onto a number of arms equal to the number of address (e.g. one address is extracted from the packet which is sent to one arm entries (outputs of 101-1 to 101-4 of Fig. 1 1 are sent via 100 to corresponding output unit 502-1 to 502-4 of Fig. 11, Araki and simultaneously conducting optical correlation processing (e.g. via 105, 107, 109 and 1 10 of Fig. 2 and via 503 and 525 of Fig. 1 1, Araki) on all arms in parallel.

Regarding claim 7, Araki in view of Holender discloses dividing an IP packet having

encoded address information (e.g. 1001 of Fig. 2 or Fig. 6, Araki) in two (e.g. one part directs to 107 and the other to 109 of Fig. 2, Araki, a step of conducting optical correlation processing (e.g. via 105, 107, 109 and 1 10 of Fig. 2 and via 503 and 525 of Fig. 1 1, Araki) to discriminate (e.g. decode) address information from an optical code in one IP packet containing address information (e.g. via 1003 of Fig. 2 or 1 16 of Fig. 4 and Col. 13, lines 14-18, Araki) between the two divided IP packets, a step of selecting an output path (e.g. via selector, 108 of Fig. 2 or 121, 1008 and 1009 of Fig. 4, Araki based on a result of the discrimination (e.g. 1005 of Fig. 2 and Col. 12, lines 40-46 or e.g. base on contention resolution, Col. 13, lines 19-44, Araki), and a step of outputting the other divided IP packet on the selected output path (e.g. 1002 of Fig. 2 switches via 100 of Fig. 1 to the output port which corresponds to its address or via 1008-1 to output unit 1 while 1005-1 goes to input unit 1, Fig. 4, Araki).

5. Claims 2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Araki in view of Holender as applied to claim 1, and further in view of U.S. Patent No. 6,473,214 B1 to Roberts et al (hereinafter Roberts).

Regarding claim 2, Araki in view of Holender discloses all limitations as discussed above, further discloses the optical encoding (e.g. via 916 of Fig. 9, Holender) is conducted by dividing an optical pulse output (e.g. via 873 of Fig. 22, Araki) by a pulse source (e.g. via 871 of Fig. 22 and Col. 5, lines 50-53, Araki) into N number of chip pulses @â2) (Col. 5, lines 61-67, Araki) and recombining (e.g. via 875 of Fig. 22, Araki) the divided optical chip pulses. He fails to discloses an optical encoding having a prescribed delay time therebetween, imparting the individual chip pulses with phase shifts of "0'. or "a'" relative to a light carrier phase of the chip pulses. Roberts discloses an optical encoder (10 of Fig. 1) having a prescribed delay time

therebetween (e.g. via 58 of Fig. 5 and Col. 12, lines 57-60), imparting the individual chip pulses with phase shifts of '.0', or "a'" (e.g. by producing zero or +/- z: phase difference) relative to the signals being combined (light carrier phase of the chip pulses) (Col. 9, lines 5-14). Accordingly, one of the ordinary in the art would have been motivated to incorporate the above delays and phase shift for producing maximum constructive and destructive interference, which could facilitate the optical signal transmission of high speed signals over long distances, with relatively low technical complexity and cost (Col. 2, lines 66-67 & Col. 3, lines 1-3). Therefore, it would have been obvious to one of artisan skill in the art to have modified the optical packet switching system of Araki in view of Holender by prescribing a delay time and imparting the individual chip pulse with phase shifts of '.0" or "a'" in the process of optical encoding because Roberts suggests that this would produce maximum constructive and destructive interference.

Regarding claim 5, Araki in view of Holender and Roberts discloses discrimination of the encoded address information (e.g. via 916 of Fig. 9, Holender) is conducted by subjecting optical chip pulses to matched filtering (e.g. via. 20 or 24 of Fig. 1, Roberts), effecting threshold processing on a center peak value (e.g. by having passband centered on the desired frequency or any desired frequency range, Col. 9, lines 51-60, Roberts) of a generated autocorrelation function (Fig. 6, Roberts), and optically regenerating the obtained "0" or "1." (e.g. maximum optical signal amplitude represents a "0" bit and a minimum optical signal amplitude represents a "1" bit, Col. 9, lines 61-67, Roberts).

6. Claims 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Araki in view of Holender as applied to claim 1, and further in view of U.S. Patent No. 6,160,656 to Mossberg et al (hereinafter Mossberg).

Regarding claim 6, Araki discloses a packet router comprising a step of optical decoding but fails to disclose that it comprises of a step of subjecting an output of an optical decoder to time gate processing, when subjecting a center peak value of a correlation function to threshold processing, thereby cutting off a center part and eliminating side-lopes of correlation waveform and a step of conducting threshold processing. Mossberg teaches the output of grating (optical decoder) (21 of Fig. 2a & Col. 4, lines 11-14) is subject to be detected by time-integrating linear or nonlinear device (time gate processing) (24a and 24b of Fig. 2a or 29a and 29b of Fig. 2b and Col. 4, lines 14-17), when subjecting a center peak value of a correlation function (e.g. 23 of Fig. 2a) to threshold processing (e.g. via threshold detection, Col. 2, lines 5-13 or via electronic thresholding device Col. 3, lines 30-34 or via by emitting a signal that is in the form of a short auto-correlation pulse, Col. 4, lines 7-45), thereby cutting off a center part and eliminating side-lopes of correlation waveform (e.g. 28 of Fig. 2b) and a step of conducting threshold processing (e.g. by setting a threshold level to discriminate between optical signals of similar energy but with and without high power subsignals, Col. 4, lines 43-64). Accordingly, one of ordinary skill in the art would have been motivated to subject the output of grating in the form of an optical decoder to time gate and threshold processing to provide a means of processing output channel signals so as to provide a robust means of differentiating between output signals of similar energy but different temporal waveform without the need of time-solving the waveform of the output signals (Col. 1, lines 60-65). Therefore, it would have been obvious to a person of

ordinary skill in the art to have modified the optical packet switching system of Araki in view of Holender by substituting the grating with an optical decoder which subjects its output to time gate and threshold processing to obtain the invention as specified in claim 6.

Regarding claim 8, Araki in view of Holender and Mossberg discloses the address information (e.g. via 912 and 916 of Fig. 9, Holender) is discriminated by sending the IP packet (e.g. 1001 of Fig. 1 1, Araki) onto a number of arms equal to the number of output paths (e.g. one address is extracted from the packet which is sent to one arm) entries (e.g. outputs of 101-1 to 101-4 of Fig. 1 1 are sent via 100 to corresponding output unit 502-1 to 502-4 of Fig. 1 1, Araki) and simultaneously conducting optical correlation processing (e.g. via 105, 107, 109 and 110 of Fig. 2 and via 503 and 525 of Fig. 1 1, Araki) on all arms in parallel.

Response to Arguments

7. Applicant's arguments filed 4/27/04 have been fully considered but they are not persuasive. The applicant contends that Araki fails to specifically teach discrimination by optical processing. However, the examiner maintains that this feature is taught by Araki in that an optical signal is processed by the system of Araki. Furthermore, see the following paragraph 8.

8. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., optical processing of the address information) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

9. In response to applicant's argument that Holender fails to specifically teach optically encoded address information usable to select an output path, a recitation of the intended use of

the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

10. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, motivation for combining the references has been provided.

11. In response to applicant's argument that the switching network of Araki would be rendered unsatisfactory for its intended purpose by the encoding system of Holender, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Agustin Bello whose telephone number is (571) 272-3026. The examiner can normally be reached on M-F 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (571)272-3022. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Agustin Bello
Examiner
Art Unit 2633

AB

M. R. Sedighian

M. R. SEDIGHIAN
PRIMARY EXAMINER